## Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

Claims 1-34 (Canceled)

Claim 35 (New): A method of manufacturing a semiconductor device comprising:

preparing a semiconductor substrate;

forming a gate first insulating layer on the semiconductor substrate;

forming a lower gate electrode layer and a cap gate layer on the gate insulating layer;

patterning the lower gate electrode layer and the cap gate layer to form a gate electrode structure;

forming an LDD region on the semiconductor substrate;

depositing an oxide layer on the gate electrode structure and the semiconductor substrate, wherein a thickness of the oxide layer is greater than a thickness of the gate insulating layer;

forming a nitride layer on the oxide layer; and

etching the oxide layer and the nitride layer to form a nitride sidewall spacer on

the gate electrode structure through the oxide layer.

Claim 36 (New): A method of manufacturing a semiconductor device according to claim 35, wherein said depositing comprises a CVD.

Claim 37 (New): A method of manufacturing a semiconductor device according to claim 35, wherein said forming a gate insulating layer comprises an oxidation.

Claim 38 (New): A method of manufacturing a semiconductor device according to claim 35, wherein the lower gate electrode layer is formed of polysilicon.

Claim 39 (New): A method of manufacturing a semiconductor device according to claim 35, wherein said etching comprises an anisotropic etching.

Claim 40 (New): A method of manufacturing a semiconductor device according to claim 35, wherein said forming a nitride layer comprises an LP-CVD.

Claim 41 (New): A method of manufacturing a semiconductor device according to claim 35, further comprising:

forming a source/drain region on the semiconductor substrate using the gate electrode structure and the nitride sidewall spacer as a mask.

Claim 42 (New): A method of manufacturing a semiconductor device according to claim 41, further comprising:

forming an intermediate insulating layer on the gate electrode structure and the semiconductor substrate;

forming a contact hole through the intermediate insulating layer so as to expose the source/drain region; and

filling a conductive material into the contact hole to form a source/drain contact electrode.

Claim 43 (New): A method of manufacturing a semiconductor device comprising:

preparing a semiconductor substrate;

oxidizing the semiconductor substrate to form a gate insulating layer on the semiconductor substrate;

forming a polysilicon layer and a metal layer on the gate insulating layer;

patterning the polysilicon layer and the metal layer to form a gate electrode structure;

forming an LDD region on the semiconductor substrate using the gate electrode structure as a mask;

depositing an oxide layer on the gate electrode structure and the semiconductor substrate, wherein a thickness of the oxide layer is greater than a thickness of the gate

insulating layer;

forming a nitride layer on the oxide layer; and

etching the oxide layer and the nitride layer to form a nitride sidewall spacer on the gate electrode structure through the oxide layer.

Claim 44 (New): A method of manufacturing a semiconductor device according to claim 43, wherein said depositing comprises a CVD.

Claim 45 (New): A method of manufacturing a semiconductor device according to claim 43, wherein said etching comprises an anisotropic etching.

Claim 46 (New): A method of manufacturing a semiconductor device according to claim 43, wherein said forming a nitride layer comprises an LP-CVD.

Claim 47 (New): A method of manufacturing a semiconductor device according to claim 43, further comprising:

forming a source/drain region on the semiconductor substrate using the gate electrode structure and the nitride sidewall spacer as a mask.

Claim 48 (New): A method of manufacturing a semiconductor device according to claim 47, further comprising:

forming an intermediate insulating layer on the gate electrode structure and the semiconductor substrate;

forming a contact hole through the intermediate insulating layer so as to expose the source/drain region; and

filling a conductive material into the contact hole to form a source/drain region contact electrode.

Claim 49 (New): A method of manufacturing a MOSFET comprising:

preparing a semiconductor substrate;

forming a gate insulating layer on the semiconductor substrate;

forming a lower gate electrode layer and a cap gate layer on the gate insulating layer;

removing a part of the lower gate electrode layer and the cap gate layer to form a gate electrode structure;

implanting ions into the semiconductor substrate using the gate electrode structure as a mask to form an LDD region on the semiconductor substrate;

depositing an oxide layer on the gate electrode structure and the semiconductor substrate by a CVD, wherein a thickness of the oxide layer is greater than a thickness of the gate insulating layer;

forming a nitride layer on the oxide layer; and

subjecting the oxide layer and the nitride layer to anisotropic etching to form a

nitride sidewall spacer on the gate electrode structure through the oxide layer.

Claim 50 (New): A method of manufacturing a MOSFET according to claim 49, wherein said forming a gate insulating layer comprises oxidation.

Claim 51 (New): A method of manufacturing a MOSFET according to claim 49, wherein the lower gate electrode layer is formed of polysilicon.

Claim 52 (New): A method of manufacturing a semiconductor device according to claim 49, wherein said forming a nitride layer comprises an LP-CVD.

Claim 53 (New): A method of manufacturing a MOSFET according to claim 49, further comprising:

implanting ions into the semiconductor substrate using the gate electrode structure and the nitride sidewall spacer as a mask to form a source/drain region on the semiconductor substrate.

Claim 54 (New): A method of manufacturing a semiconductor device according to claim 53, further comprising:

forming an intermediate insulating layer on the gate electrode structure and the semiconductor substrate;

forming a contact hole through the intermediate insulating layer so as to expose the source/drain region; and

filling a conductive material into the contact hole to form a source/drain contact electrode.